

App. No. 09/700,940
Office Action Dated July 28, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Claims 1 and 6 are amended.

Claim 8 is new.

Listing of Claims:

1. (Currently Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of:
 - providing a power supply capacitor cell corresponding to a logic gate cell, a capacitance value of the power supply capacitor cell being determined based on a drive load capacity value of the logic gate cell, and
 - arranging the power supply capacitor cell in a vicinity of the logic gate cell used to determine the capacitance value of the power supply capacitor cell after the capacitance value is determined in the providing step, so as to connect a power supply line of the logic gate cell with a ground line of the logic gate cell through the power supply capacitor cell.
2. (Previously Presented) The LSI layout method according to claim 1, wherein the capacitance value of the power supply capacitor cell is determined to be substantially twice as large as the drive load capacity value of the logic gate cell.
3. (Previously Presented) The LSI layout method according to claim 1, wherein the power supply capacitor cell is arranged in the vicinity of the logic gate cell which changes simultaneously with clock synchronization.
4. (Previously Presented) A LSI layout method according to claim 1, further comprising the operations of:
 - calculating a possible number of the power supply capacitor cells to be arranged based on a width of a dead space of the power supply and a width of the power supply capacitor cells,

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and

arranging the power supply capacitor cells in spaces of each block where standard cells are not arranged by the automatic arrangement wiring.

5. (Previously Presented) The LSI layout method according to claim 1, wherein the power supply capacitance cell includes:

- a p-sub wafer;
- a n-well fixed to the ground line on the p-sub wafer, and
- a polysilicon gate fixed to the power supply line on the n-well.

6. (Currently Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of:

providing a power supply capacitor cell corresponding to a logic gate cell, a capacitance value of the power supply capacitor cell being determined based on a drive load capacity value of the logic gate cell, and

arranging the power supply capacitor cell adjacent to the logic gate cell used to determine the capacitance value of the power supply capacitor cell after the capacitance value is determined in the providing step, so as to connect a power supply line of the logic gate cell with a ground line of the logic gate cell through the power supply capacitor cell.

7. (Previously Presented) The LSI layout method according to claim 1, wherein prior to providing a power supply capacitor cell to a corresponding logic gate cell, a plurality of logic gate cells are automatically arranged.

8. (New) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operation of:

- estimating a drive load capacity of a logic gate cell;
- providing a power supply capacitor cell corresponding to the logic gate cell,
- determining a capacitance value of the power supply capacitor cell based on the drive load capacity estimated in the estimating step, and
- arranging the power supply capacitor cell when an automatic arrangement is executed

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such that the power supply capacitor cell is placed in a vicinity of the logic gate cell used to determine the capacitance value of the power supply capacitor cell,
wherein the arrangement step is executed after the determining step.

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